AMENDMENTS TO THE SPECIFICATION:

Please amend paragraph [0006] beginning at page 4, line 15, and continuing to page 5, line 18, as follows:

Figs. 13 and 14 show sectional views of typical ~~GTO's~~ GTOs of the second and third background art using SiC, respectively. In the second background art GTO shown in Fig. 13, a lightly doped p-type SiC base layer 2 is formed on a heavily doped n-type SiC cathode emitter layer 1 that has a cathode electrode 21 connected to a cathode terminal K (hereinafter referred to as a cathode K) on its lower surface. An n-type base layer 3 is formed on the p-type base layer 2. A p-type layer, a central region of which is left and becomes a p-type anode emitter layer 4 in a subsequent process, is formed by the epitaxial growth method on the entire surface of the n-type base layer 3. Next, the mesa-type anode emitter layer 4 is formed by etching away a region of the p-type layer other than a region that becomes the anode emitter layer 4 by the reactive ion etching method until the surface of the n-type base layer 3 is somewhat removed. An n-type gate contact region 6 is formed by ion implantation so as to surround the anode emitter layer 4 in a portion located apart from a junction J of the end portion of the exposed n-type base layer 3. An anode electrode 20 connected to an anode terminal A (hereinafter referred to as an anode A) is formed on the anode emitter layer 4, and a gate electrode 22 connected to a gate terminal G (hereinafter referred to as a gate G) is formed on the gate contact region 6. Finally, in order to prevent moisture and ions ~~of~~ such as Na ions and the like from adhering to the surface of the GTO, an insulator 10 of silicon dioxide (SiO_2) or the like is formed on the entire surface excluding the electrodes.

Please amend the paragraph beginning at page 5, line 24, and continuing to page 6, line 5, as follows:

In the GTO shown in Fig. 13, an off-gate voltage is applied between the gate G and the anode A at the turn-off time. Moreover, in the GTO shown in Fig. 14, an off-gate voltage is applied between the cathode K and the gate G at the turn-off time. As a result, the principal current is diverted into the gate G to turn off the GTO both in the GTOs~~GTO's~~ of Figs. 13 and 14.

Please amend the caption on page 10, line 22, as follows:

BRIEF SUMMARY ~~OF THE INVENTION~~

Please amend paragraph [0018] beginning at page 10, line 23, and continuing to page 11, line 5, as follows:

According to the technology disclosed herein~~present invention~~, in the gate turn-off thyristor (hereinafter referred to as a wide-gap GTO) of a wide-gap semiconductor that has a mesa-type emitter layer, the maximum controllable current is increased by relieving the electric field of the insulator located in the neighborhood of the end portion of the junction between an emitter layer and a base layer where a gate is provided adjacent to the emitter layer.

Please amend paragraphs [0020] - [0025] beginning at page 12, line 6, and continuing to page 17, line 15, as follows:

A gate turn-off thyristor of a wide-gap semiconductor of an example embodiment~~the present invention~~ includes a first emitter layer of either one of n-type and p-type conductive types having a first electrode on its one surface and a first base layer of a conductive type different from that of the first emitter layer provided on the other surface of the first emitter layer. This gate turn-off thyristor further includes a second base layer of a conductive type identical to that of the first emitter layer provided on the first base layer, a mesa-type second emitter layer of a conductive type different from that of the first emitter layer provided on the second base layer and a second electrode provided on the mesa-type second emitter layer. A low-resistance gate region is provided so as to surround the mesa-type second emitter layer in a region located apart from an end portion of a junction between the mesa-type second emitter layer and the second base layer, formed in a region that extends from a neighborhood of the end portion of the junction to a bottom portion of the mesa-type second emitter layer with interposition of the second base layer between the region and the junction, and having a conductive type identical to that of the second base layer and an impurity concentration higher than that of the second base layer. A third electrode is put in contact with an end portion of the low-resistance gate region.

According to the technology disclosed herein~~present invention~~, by virtue of the first conductive type low-resistance gate region formed in the first conductive type base

layer, an electron current flows from the first conductive type base layer through the first conductive type low-resistance gate region and the first conductive type gate contact region to the gate at the turn-off time. Since the low-resistance gate region has a low resistance value, a voltage drop in the first conductive type base layer is small even when a current due to the electron flow is large. Therefore, the off-gate voltage applied between the anode and the gate is not influenced by the voltage drop, and a large current can be flowed with high efficiency. As a result, the controllable current of the GTO can be increased.

In another aspect of the technology disclosed herein~~present invention~~, a gate turn-off thyristor of a wide-gap semiconductor includes a first emitter layer of either one of n-type and p-type conductive types having a first electrode on its one surface and a first base layer of a conductive type different from that of the first emitter layer provided on the other surface of the first emitter layer. This GTO further includes a second base layer of a conductive type identical to that of the first emitter layer provided on the first base layer and a mesa-type second emitter layer of a conductive type different from that of the first emitter layer provided on the second base layer. This GTO further includes a second electrode, which is put in contact with a central region of the mesa-type second emitter layer and put in contact with the second emitter layer via a contact electrode in a region excluding the central region of the second emitter layer. In a region located apart from the end portion of the junction between the mesa-type second emitter layer and the second base layer, a low-resistance region, which has a conductive type identical to that of the second base layer and an impurity concentration higher than that of the second base layer, is provided so as to surround the mesa-type second emitter layer. A third electrode is provided in contact with the end portion of the low-resistance region.

In another aspect of the technology disclosed herein~~present invention~~, a gate turn-off thyristor of a wide-gap semiconductor includes a first emitter layer of either one of n-type and p-type conductive types having a first electrode on its one surface, a first base layer of a conductive type different from that of the first emitter layer provided on the other surface of the first emitter layer, a second base layer of a conductive type identical to that of the first emitter layer provided on the first base layer, a mesa-type second emitter layer of a conductive type different from that of the first emitter layer provided on the second base layer, a high-resistance region provided in a central region of an upper surface of the second emitter layer and having a conductive type identical to that of the

second emitter layer and an impurity concentration lower than that of the second emitter layer, a contact electrode put in contact with the second emitter layer and the high-resistance region, a second electrode put in contact with the contact electrode and the second emitter layer at least at a peripheral portion of the contact electrode, and having a contact resistance to the emitter layer greater than a contact resistance of the contact electrode to the emitter layer, a low-resistance region provided so as to surround the mesa-type second emitter layer in a region located apart from an end portion of a junction between the mesa-type second emitter layer and the second base layer, and having a conductive type identical to that of the second base layer and an impurity concentration higher than that of the second base layer, and a third electrode put in contact with an end portion of the low-resistance region.

According to the technology disclosed herein~~present invention~~, the second electrode is put in contact with only the central region of the second emitter layer and put in contact with the second emitter layer via the contact electrode formed of a material of which the contact resistance to the semiconductor layer is lower than that of the second electrode in the other region. Therefore, the contact resistance between the second electrode and the second emitter layer in the region located with interposition of the contact electrode is lower than that of the other region. With this arrangement, a current that flows from the second electrode into the second emitter layer flows more in the peripheral region located with interposition of the contact electrode than in the central region where the resistance is relatively high. In the GTO, the current control effect by virtue of the low-resistance region is great in a portion located near the low-resistance region, but the effect is reduced in the central region remote from the low-resistance region. In ~~the present invention~~an example embodiment, the greater part of the electrification current is flowed in the peripheral region where the current control effect by virtue of the low-resistance region is high, so that the current in the central region of a low control effect is reduced. As a result, the efficiency of extracting a current from the gate at the turn-off time is increased, and therefore, the controllable current of the GTO is increased.

According to ~~the present invention~~an example embodiment, by sufficiently separating the gate contact region of the GTO that uses a wide-gap semiconductor from the junction between the mesa-type emitter layer and the base layer, the electric field in the neighborhood of the junction or in the neighborhood of the mesa corner portion is not

increased even when the off-gate voltage is high. By raising the off-gate voltage, the current flowing between the anode and the cathode can efficiently be diverted into the gate, and the controllable current of the GTO can be increased. Moreover, since a high electric field is not applied to the insulator, the leakage current is not increased, and the long-term reliability can be maintained.

Please amend paragraphs [0027] - [0038] beginning at page 18, line 10, and continuing to page 19, line 13, as follows:

Fig. 1 is a top view of a gate turn-off thyristor of a first example embodiment ~~of the present invention~~;

Fig. 2 is a sectional view of ~~the~~a gate turn-off thyristor of ~~the~~a first example embodiment ~~of the present invention~~;

Fig. 3 is a sectional view of ~~the~~a gate turn-off thyristor of ~~the~~a second example embodiment ~~of the present invention~~;

Fig. 4 is a sectional view of ~~the~~a gate turn-off thyristor of ~~the~~a third example embodiment ~~of the present invention~~;

Fig. 5 is a sectional view of ~~the~~a gate turn-off thyristor of ~~the~~a fourth example embodiment ~~of the present invention~~;

Fig. 6 is a sectional view of ~~the~~a gate turn-off thyristor of ~~the~~a fifth example embodiment ~~of the present invention~~;

Fig. 7 is a sectional view of ~~the~~a gate turn-off thyristor of ~~the~~a sixth example embodiment ~~of the present invention~~;

Fig. 8 is a sectional view of ~~the~~a gate turn-off thyristor of ~~the~~a seventh example embodiment ~~of the present invention~~;

Fig. 9 is a sectional view of ~~the~~a gate turn-off thyristor of ~~the~~a eighth example embodiment ~~of the present invention~~;

Fig. 10 is a sectional view of ~~the~~a gate turn-off thyristor of ~~the~~a ninth example embodiment ~~of the present invention~~;

Fig. 11 is a sectional view of ~~the~~a gate turn-off thyristor of ~~the~~a tenth example embodiment ~~of the present invention~~;

Fig. 12 is a sectional view of ~~the~~a gate turn-off thyristor of ~~the~~a eleventh example embodiment ~~of the present invention~~;

Please amend paragraphs [0041] - [0042] beginning at page 20, line 18, and continuing to page 22, line 21, as follows:

Preferred embodiments of the gate turn-off thyristor (hereinafter, abbreviated to GTO) that uses silicon carbide (hereinafter, SiC) of the technology disclosed hereinpresent invention will be described with reference to Figs. 1 through 12. Fig. 1 is a top view of one element of the GTO of the first example embodiment of the present invention. Figs. 2 through 8 are sectional views of one element (unit) of the GTO of each embodiment exampleof the present invention. No hatching is shown in the cross sections of the figures for the sake of clear views of the figures. The top views of the GTOsGTO's of the embodiments are basically similar to the one shown in Fig. 1. In the actual construction of the GTO of each of the embodiments, a number (normally several tens to several thousands) of elements are connected together on an identical substrate horizontally in the figure, and the anode electrodes, gate electrodes and cathode electrodes are connected parallel or in series depending on the situation. Although not shown in the figures, it is general thattypically a number of elements are horizontally arranged and a number of elements are also arranged in columns in the vertical direction in the figures.

FIRST EMBODIMENT

A GTO that uses SiC of the first example embodiment of the present invention is described with reference to Figs. 1 and 2. Fig. 1 is a top view that shows the upper surface before the provision of an insulator 10 of the GTO of the first embodiment. Fig. 2 is a sectional view taken along the line II-II of Fig. 1. In Figs. 1 and 2, the GTO of the present embodiment has a heavily doped cathode emitter layer 1 (first emitter layer) of an n-type (first conductive type) SiC semiconductor that has a thickness of about 350 μm and an impurity concentration of not smaller than about 10^{19} cm^{-3} and is provided with a cathode electrode 21 (first electrode) connected to the cathode terminal K (cathode K, hereinafter). A lightly doped base layer 2 (first base layer) of a p-type (second conductive type) SiC semiconductor that has a thickness of 50 μm and an impurity concentration of about 10^{16} to 10^{13} cm^{-3} is formed on the cathode emitter layer 1. A thin n-type base layer 3 (second base layer) of a thickness of several micrometers is formed on the p-type base layer 2. A p-type layer that serves as a p-type anode emitter layer 4 is grown by the epitaxial growth method on the entire surface of the n-type base layer 3

leaving a central region in a subsequent process. A flat interface is formed between the p-type anode emitter layer 4 (the second emitter layer) and the n-type base layer 3 (the second base layer). Next, a mesa-type anode emitter layer 4 is formed by deeply etching the other region by the reactive ion etching method to an extent that the surface of the n-type base layer 3 is exposed and its surface portion is somewhat removed leaving a region that becomes the p-type anode emitter layer 4 (second emitter layer). By implanting ions into the exposed surface n-type base layer 3, an n-type low-resistance gate region 5 and an n-type gate contact region 6 are successively formed so as to surround the anode emitter layer 4. The impurity concentration of the low-resistance gate region 5 should preferably be three times the impurity concentration of the base layer 3. The low-resistance gate region 5 may be formed down to the neighborhood of the upper surface of the base layer 2 in the ion implantation process. The low-resistance gate region 5 is formed slightly apart from the junction J between the anode emitter layer 4 and the base layer 3. As shown in Fig. 2, low-resistance gate region 5 is thus embedded in the second base layer 3 below the interface or junction J and spaced away from the interface in a stacking direction (i.e., the stacking direction being perpendicular to the interface or junction J). The gate contact region 6 is a low-resistance region of an impurity concentration higher than that of the low-resistance gate region 5 and is formed in a position located far apart from the junction J. An anode electrode 20 (second electrode) connected to an anode terminal A (anode A, hereinafter) is formed on the anode emitter layer 4, and a gate electrode 22 (third electrode) connected to a gate terminal G (gate G, hereinafter) is formed on the gate contact region 6. Finally, in order to prevent moisture and ions of Na ions and the like from adhering to the surface of the GTO after the formation of the layers, an insulator 10 of silicon dioxide (SiO_2) or the like is formed on the entire surface excluding the electrodes. Nitrogen can be used as an n-type impurity. Moreover, boron and aluminum can be used as a p-type impurity. From Fig. 2 it can be seen that a region or volume comprising the second base layer 3 has homogeneous impurity concentration, such region extending between the interface of the second base layer 3 and the second emitter layer 4 on its top and a lower layer upon which the second base layer 3 is formed.

Please amend paragraph [0051] beginning at page 27, line 21, and continuing to page 29, line 2, as follows:

Fig. 3 is a sectional view of a GTO that uses SiC of ~~the~~ a second example embodiment ~~of the present invention~~. In Fig. 3, the p-type and the n-type of the layers are interchanged in the GTO of the present embodiment in comparison with the GTO of the first embodiment shown in Fig. 2. A lightly doped n-type SiC base layer 2 (second base layer) that has a thickness of about 50 μm is formed on the upper surface of a p-type anode emitter layer 4A (first emitter layer) that has a thickness of about 350 μm and is provided with an anode electrode 20 (first electrode) connected to the anode A on its lower surface. A thin p-type base layer 3A (second base layer) that has a thickness of several micrometers is formed on the base layer 2A, and an n-type layer of which central region is left in a subsequent process to serve as an n-type cathode emitter layer 1A is formed by the epitaxial growth method on the entire surface of the p-type base layer 3A. Next, a region is deeply etched by the reactive ion etching method to an extent that the surface of the p-type base layer 3A is exposed and its surface portion is somewhat removed leaving the other region that becomes the cathode emitter layer 1A (second emitter layer) of the n-type layer, forming the mesa-type cathode emitter layer 1A. Then, the cathode electrode 21 (second electrode) is formed on the cathode emitter layer 1A. A low-resistance gate region 5A that has a p-type high impurity concentration by ion implantation and a low resistance and a p-type gate contact region 6A are formed successively layered on the exposed p-type base layer 3A so as to surround the cathode emitter layer 1A. A gate electrode 22 (third electrode) is formed on the gate contact region 6A. Finally, an SiO_2 insulator 10 is formed on the entire surface excluding the electrodes.

Please amend paragraph [0054] beginning at page 30, line 12, and continuing to page 31, line 15, as follows:

Fig. 4 is a sectional view of a GTO that uses SiC of ~~the~~ a third example embodiment ~~of the present invention~~. In the GTO of the present embodiment shown in the figure, a p-type region 7, which includes at least the neighborhood of the end portion of the junction J between the p-type anode emitter layer 4 and the n-type base layer 3 and expands from the neighborhood of a corner portion MC of the mesa M toward the gate electrode 22, is formed in the n-type base layer 3. The other construction is the same as that of the GTO of the first embodiment shown in Fig. 2. By virtue of the formation of the p-type region 7, the field intensity of the insulator 10 in the neighborhood of the mesa

corner portion MC located at the end portion of the junction J between the p-type anode emitter layer 4 and the n-type base layer 3 can be relieved even when the off-gate voltage at the turn-off time is increased. As a result, the withstand voltage between the gate G and the anode A can be raised, and the controllable current can be increased. Moreover, since the intensity of the electric field applied to the insulator 10 can be reduced, the deterioration of the insulator 10 can be prevented. Therefore, an increase in the leakage current between the gate G and the anode A is not caused even during a long-term use, and high reliability can be maintained for a long term. In the concrete example of the GTO of the present embodiment, the withstand voltage between the gate G and the anode A was 205 V, which means that a withstand voltage higher than the withstand voltage (150 V) of the GTO of the first embodiment was able to be obtained.

Please amend paragraph [0055] beginning at page 31, line 18, and continuing to page 33, line 10, as follows:

Fig. 5 is a sectional view of a GTO that uses SiC of ~~the~~ a fourth example embodiment ~~of the present invention~~. In the GTO of the present embodiment shown in the figure, the n-type low-resistance gate region 5 is provided in a portion of an end region of the n-type base layer 3 excluding the p-type anode emitter layer 4. The n-type low-resistance gate region 5 is formed by self-alignment in the n-type base layer 3 by means of a mask for mesa etching for forming the p-type anode emitter layer 4. Therefore, a process for forming the pattern of the n-type low-resistance gate region 5 can be eliminated. In the present embodiment, as in the third embodiment, a p-type region 7, which includes at least the neighborhood of the end portion of the junction J between the p-type anode emitter layer 4 and the n-type base layer 3 and expands from the neighborhood of the corner portion MC of the mesa M to the gate electrode 22, is formed in the n-type low-resistance gate region 5. The other construction is the same as that of the first embodiment shown in Fig. 2. The formation of the p-type region 7 prevents the formation of a junction between the heavily doped p-type anode emitter layer 4 and the heavily doped n-type low-resistance gate region 5 in the neighborhood of the mesa corner portion MC and forms a junction at the bottom surface of the mesa M. As a result, the field intensity of the insulator 10 in the neighborhood of the mesa corner portion MC is relieved, and the off-gate voltage can be raised. It is also acceptable to enlarge the p-type region 7 so that the region covers the mesa corner portion MC and

form the region connected to the anode emitter layer 4. According to the concrete example of the present embodiment, the withstand voltage between the gate G and the anode A was 130 V, which means that a withstand voltage remarkably higher than the withstand voltage (about 30 V) of the conventional GTO was able to be obtained although the withstand voltage is lower than the withstand voltage (150 V) of the GTO of the first embodiment. Since the withstand voltage is high, the controllable current can be increased by raising the gate voltage. In the GTO of the present fourth embodiment, the gate contact region 6A, which is provided in the GTO of each of the first through third embodiments, is not provided. Therefore, the construction is simple, and the manufacturing cost is low.

Please amend paragraph [0056] beginning at page 33, line 13, and continuing to page 34, line 3, as follows:

Fig. 6 is a sectional view of a GTO that uses SiC of ~~the~~ a fifth example embodiment ~~of the present invention~~. In Fig. 6, the GTO of the present embodiment has a construction in which the n-type low-resistance gate region 5 is excluded from the GTO of the third embodiment shown in Fig. 4. In a process for forming the n-type low-resistance gate region 5 in the GTO of the third embodiment, a heavily doped n-type layer is formed by carrying out ion implantation into the n-type base layer 3. At this time, crystal defects easily occur in the n-type base layer 3 and the n-type low-resistance gate region 5. As a result, a leakage current on a surface between the gate and the anode is increased. Since the n-type low-resistance gate region 5 is not provided in the present embodiment, the problem caused by the crystal defects does not occur in the n-type base layer 3.

Please amend paragraph [0058] beginning at page 35, line 2, and continuing to page 36, line 14, as follows:

Fig. 7 is a sectional view of a GTO that uses SiC of ~~the~~ a sixth example embodiment ~~of the present invention~~. In the GTO of the present embodiment, a p-type base layer 2 is formed by the epitaxial growth method on a heavily doped n-type SiC cathode emitter layer 1 provided with a cathode electrode 21 on its lower surface. Next, an n-type low-resistance gate region 5 is formed in both end regions of the p-type base layer 2. Next, an n-type base layer and a p-type anode emitter layer, which become the n-

type base layer 3 and the p-type anode emitter layer 4, respectively, through a subsequent process, are successively layered by the epitaxial growth method on the entire surfaces of the p-type base layer 2 and the n-type low-resistance gate region 5, respectively. Both the end regions of the n-type base layer and the p-type anode emitter layer are etched by the reactive ion etching method until the surface of the n-type low-resistance gate region 5 is exposed, forming the mesa-type n-type base layer 3 and p-type anode emitter layer 4 that have a mesa slope MS. According to the construction of the present embodiment, a junction JE exposed on the mesa slope MS of the p-type anode emitter layer 4 and the n-type base layer 3 is separated from the neighborhood of the mesa corner portion MC where electric field concentration easily occurs, allowing a sufficient creeping distance to be provided. Therefore, since the off-gate voltage can be raised, a GTO of a large controllable current can be provided. When the n-type low-resistance gate region 5 is formed in the n-type base layer 3 by implanting ions to a deep portion in the base layer 3 as in the cases of the first through fourth embodiments, crystal defects easily occur in the n-type base layer 3. In contrast to this, when the n-type base layer 3 is formed by the reactive etching method, no crystal defect occurs in the n-type base layer 3. Since the ion implantation is carried out only in forming the n-type low-resistance gate region 5 in the p-type base layer 2, ion implantation processes are few, and the manufacturing processes of the GTO can be simplified.

Please amend paragraphs [0060] - [0061] beginning at page 37, line 1, and continuing to page 38, line 4, as follows:

Fig. 8 is a sectional view of a GTO that uses SiC of ~~the~~ a seventh example embodiment ~~of the present invention~~. In the GTO of the present embodiment, at least one n-type low-resistance gate small region 55 is formed in the neighborhood of the surface of the p-type base layer 2 within an active region where a principal current flows between the n-type low-resistance gate regions 5 located at both end portions. The other construction is the same as that shown in Fig. 7. In the GTO of the present embodiment, the greater part of the flow of electrons injected from the n-type cathode emitter layer 1 into the p-type base layer 2 at the turn-off time can effectively be diverted into the right and left gate electrodes 22 by the n-type low-resistance gate region 55 formed in the active region. With this arrangement, a GTO of a large controllable current can be provided. Even if the lifetime of the carriers (electrons and holes) becomes long at high

temperature when the use temperature exceeds 150°C or when the amount of holes that pass through the n-type base layer 3 and flows into the p-type base layer 2 are increased as a consequence of an increase in the hole density due to an increase in the ionization rate of the p-type anode emitter layer 4, the controllable current is scarcely reduced.

The technology disclosed herein~~present invention~~ can also be applied to GTO's that are constituted by interchanging the n-type layers and regions with p-type layers and regions and interchanging the p-type layers and regions with n-type layers and regions in the first through seventh embodiments.

Please amend paragraph [0062] beginning at page 38, line 7, and continuing to page 39, line 14, as follows:

Fig. 9 is a sectional view of a GTO that uses SiC of ~~the~~ an eighth example embodiment~~ of the present invention~~. In the figure, an anode contact electrode 61 is formed in a region excluding the center portion of the upper surface of the mesa-type anode emitter layer 4. An anode electrode 60 connected to the anode A is put in contact with only the central region of the anode emitter layer 4. In a peripheral region excluding the central region of the anode emitter layer 4, the anode electrode 60 is put in contact with the anode emitter layer 4 via the anode contact electrode 61. Nickel is used for the anode contact electrode 61, and gold, of which the contact resistance to the semiconductor layer is higher than nickel, is used for the anode electrode 60. In the present technical field, it is known that, when a metal film is formed on an SiC semiconductor layer, a contact resistance between the two is varied depending on the kind of the metal and heat treatment after the film formation of the metal film besides the electrical conductivity of the metal. Metals of a low contact resistance include nickel, titanium, aluminum, tungsten and composite films of these metals. Metals of a high contact resistance include gold and so on. In the present embodiment, the anode contact electrode 61 of nickel is provided divided into at least right and left two regions and subjected to appropriate heat treatment. A gap between the anode contact electrodes 61 located in the two regions is about 1 μm to 20 μm. The other construction is similar to that of the fifth embodiment shown in Fig. 6. Although an angle between the side surface of the mesa-type anode emitter layer 4 and the surface of the base layer 3 is about 90 degrees in Fig. 9, the present embodiment is also applicable even when the angle is within a range of about 140 degrees to 50 degrees.

Please amend paragraph [0066] beginning at page 40, line 24, and continuing to page 42, line 4, as follows:

Fig. 10 is a sectional view of a GTO that uses SiC of ~~the~~ a ninth example embodiment ~~of the present invention~~. In ~~the figure~~Fig. 10, an anode contact electrode 71 of a material of a low contact resistance such as nickel is formed on the anode emitter layer 4. A lightly doped p-type region 73 is provided in the central region of the surface of the anode emitter layer 4. An anode electrode 70 is formed on the anode contact electrode 71. The anode electrode 70 is made larger than the anode contact electrode 71, and its end portion is put in direct contact with a peripheral portion of the anode emitter layer 4. The other construction is similar to that of the eighth embodiment. Since the p-type region 73 has a low impurity concentration, a contact resistance between the region 73 and the anode contact electrode 71 is high. Moreover, the internal resistance of the region 73 is also higher than the peripheral anode emitter layer 4. As a result, Hall current flows while being diverted to the right and left going around the center portion, as in the eighth embodiment. Therefore, the electron current also flows while being diverted into the right and left. The region, where electrons exist in surplus due to the diverted electron flows, comes close to the gate contact region 6. Therefore, the electron density is reduced in the central region of the p-type base layer 2. As a result, electrons can efficiently be extracted from the gate, and therefore, the controllable current is increased. Although the angle between the side surface of the mesa-type anode emitter layer 4 and the surface of the base layer 3 is about 90 degrees in Fig. 10, the present embodiment is also applicable even when the angle is within a range of about 140 degrees to 50 degrees.

Please amend paragraph [0067] beginning at page 42, line 7, and continuing to page 42, line 24, as follows:

Fig. 11 is a sectional view of a GTO that uses SiC of ~~the~~ a tenth example embodiment ~~of the present invention~~. The GTO of the present embodiment differs from that of the ninth embodiment in that a heavily doped n-type region 83 is formed in place of the lightly doped p-type region 73. The other construction is similar to that of the ninth embodiment shown in Fig. 10. Also, in the construction, a current scarcely flows in the central region of the anode emitter layer 4, and Hall current flows while being

diverted into the right and left in the anode emitter layer 4. Therefore, an electron current also flows while being diverted into the right and left regions. As a result, the paths of the diverted electron flows come close to the gate contact region 6. Therefore, the control efficiency is improved, and the controllable current is improved. The n-type region 83 can be concurrently formed by ion implantation when the gate contact region 6 is formed, and therefore, the formation processes become simplified.

Please amend paragraph [0068] beginning at page 43, line 2, and continuing to page 43, line 14, as follows:

Fig. 12 is a sectional view of a GTO that uses SiC of ~~the~~ an eleventh example embodiment ~~of the present invention~~. In the present embodiment, a heavily doped n-type region 93 is provided in a central region of the surface of the n-type base layer 3. The other construction is similar to that of the ninth embodiment shown in Fig. 10. In the construction, the flow of Hall current, which flows from the anode emitter layer 4 toward the cathode emitter layer 1, is disturbed by the n-type region 93 formed in the central region of the base layer 3 and diverted into the right and left in the base layer 3. As a result, the controllable current can be increased by an effect similar to that of the eighth embodiment

Please amend paragraph [0069] beginning at page 43, line 17, and continuing to page 43, line 20, as follows:.

The technology disclosed herein~~present invention~~ can be used for the gate turn-off thyristor that uses a wide-gap semiconductor capable of interrupting a large current within a wide temperature range.